High-Speed Pipelined ADCs

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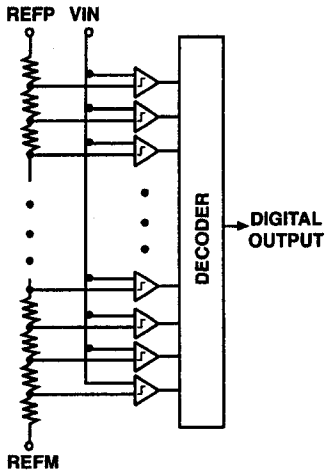
Outline

N-Bit Flash ADC



+ Fastest Architecture

- Requires 2^N comparators

- All comparators N-bit accurate

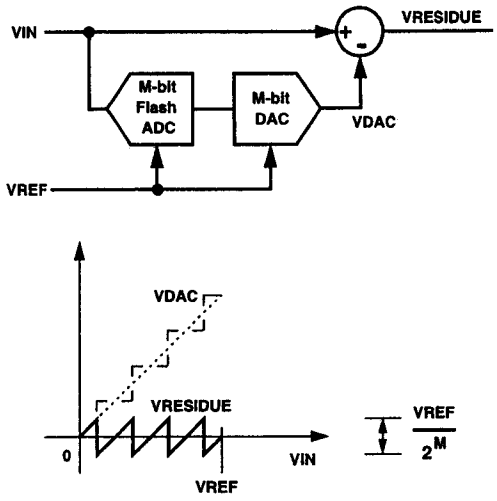
ADC Architectural Goals

1) Reduce number of comparators

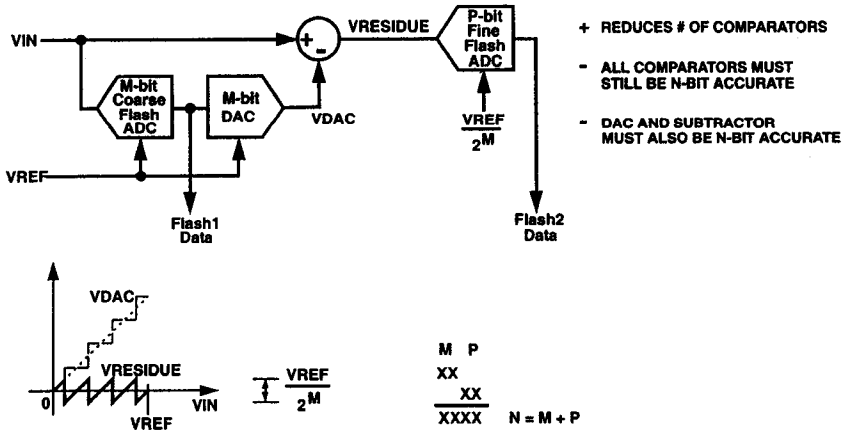
2) Reduce accuracy requirements of comparators

3) Maintain high conversion rate

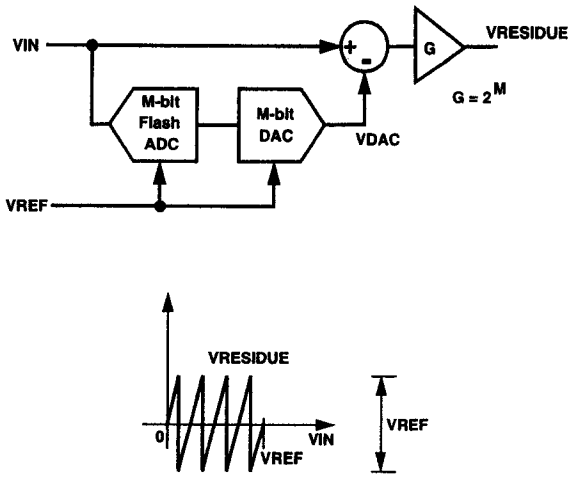
Residue Circuit



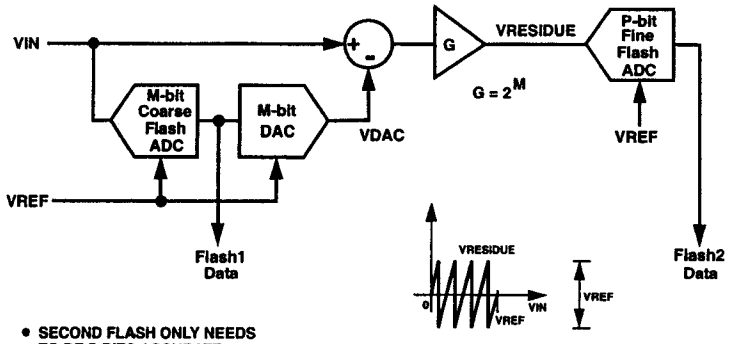
Two-Step Architecture



Amplified Residue



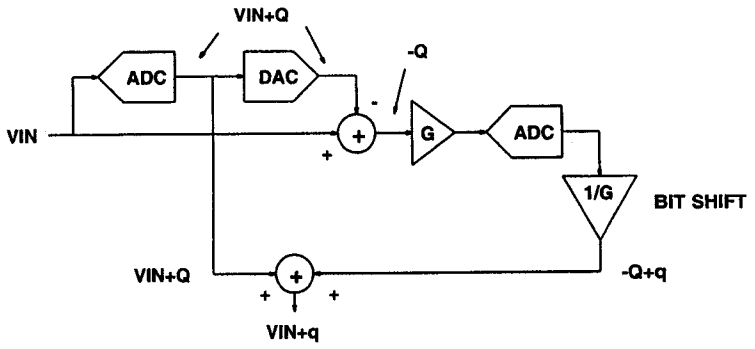
N-bit Two-Step with Interstage-Gain



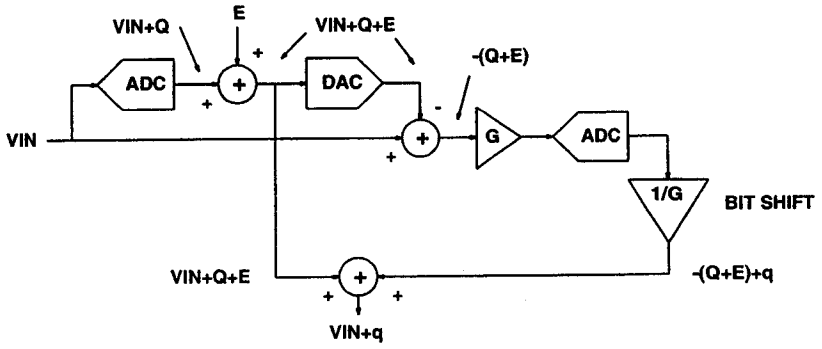
- SECOND FLASH ONLY NEEDS TO BE P BITS ACCURATE
- FIRST FLASH MUST STILL BE N BITS ACCURATE
- DAC AND SUBTRACTOR MUST BE N BITS ACCURATE
- GAIN BLOCK ONLY NEEDS TO BE N-M BITS ACCURATE

M P
XX
XX
XXXX M + P bit Output

Block Diagram Analysis of Two-Step Operation

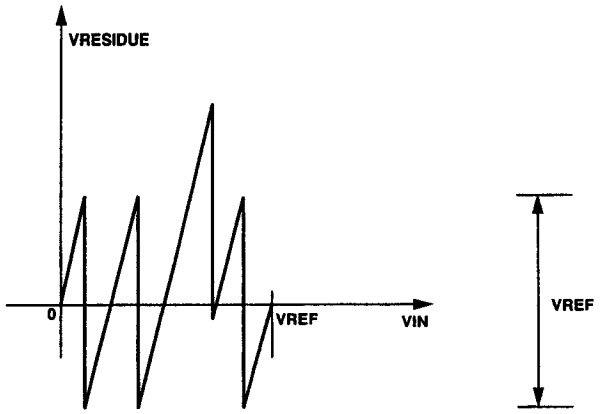


Correction of Errors in First-Stage Flash

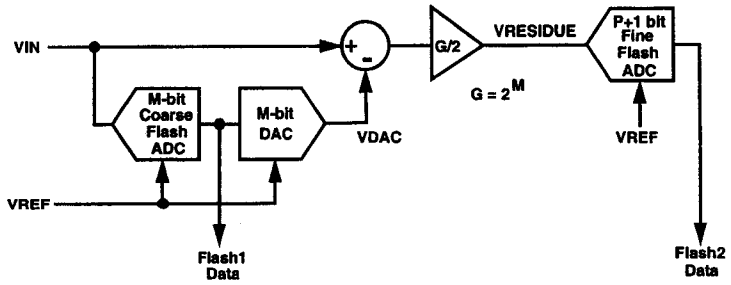


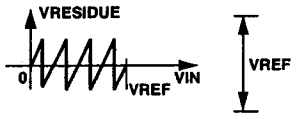
- **Error correction requires additional dynamic range in second-stage flash**

Effect of Flash1 Error on Residue Signal



Modifications to Allow Correction of Flash1 Errors

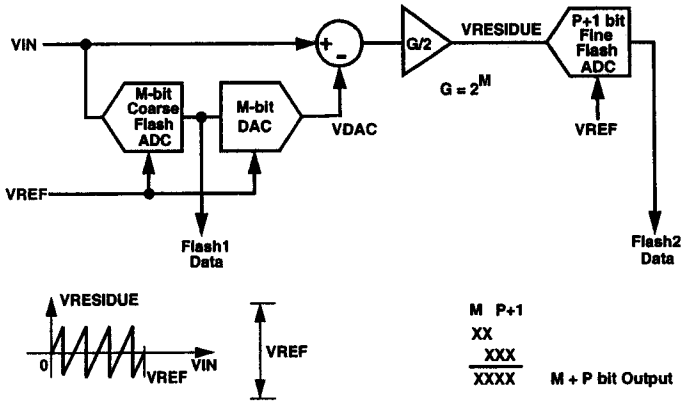




M P+1
XX
XXX
XXXX M + P bit Output

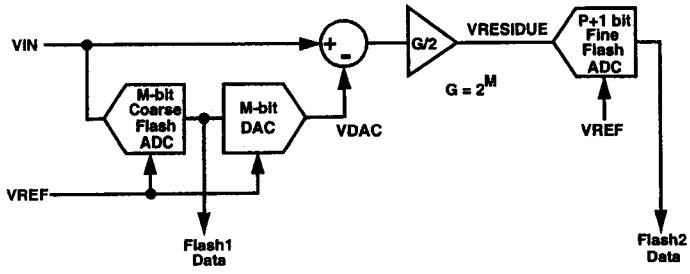
- Decrease Interstage Gain
- Increase Resolution of Flash2

Two-Step with Interstage Gain & Flash Overlap Correction



- Interstage Gain Reduces Accuracy Requirements of Second-Stage
- First Stage Errors Corrected by Second Stage with Overlap Correction

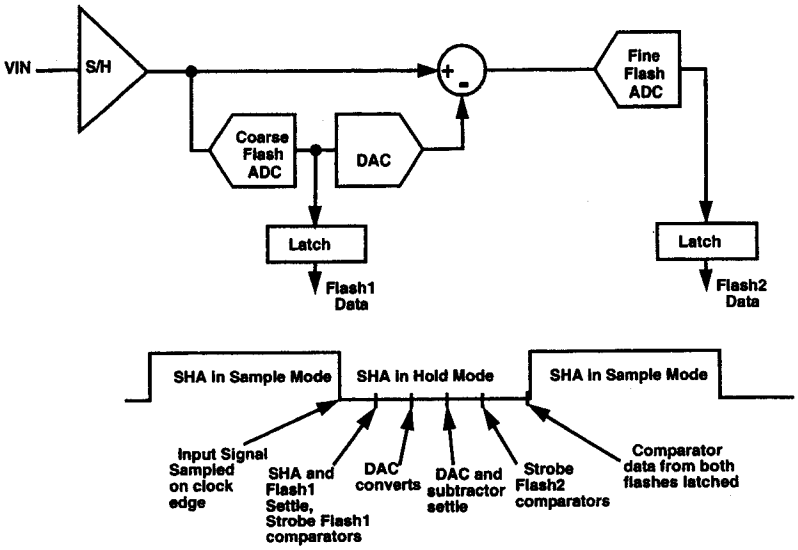
Accuracy Requirements



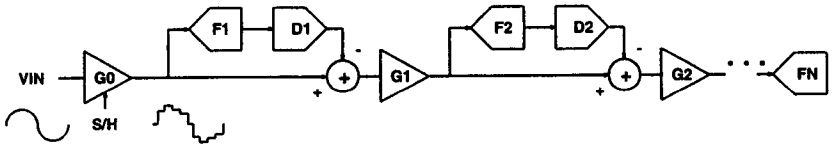
\+ NEITHER FLASH NEEDS N BIT ACCURACY
\+ FIRST FLASH ONLY M BITS ACCURATE
\- SECOND FLASH ONLY P+1 BITS ACCURATE
\- DAC AND SUBTRACTOR N BITS ACCURATE
\- GAIN BLOCK ONLY N-M+1 BITS ACCURATE

M P+1
XX
XXX
XXXX
M + P bit Output

Two-Step Timing

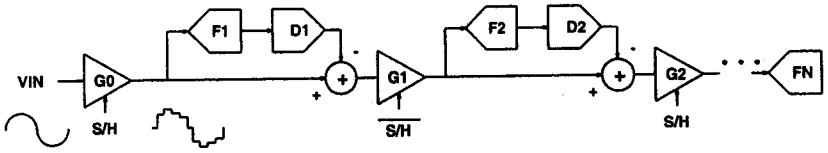


Multi-Step Architecture (e.g. AD1671,1990)



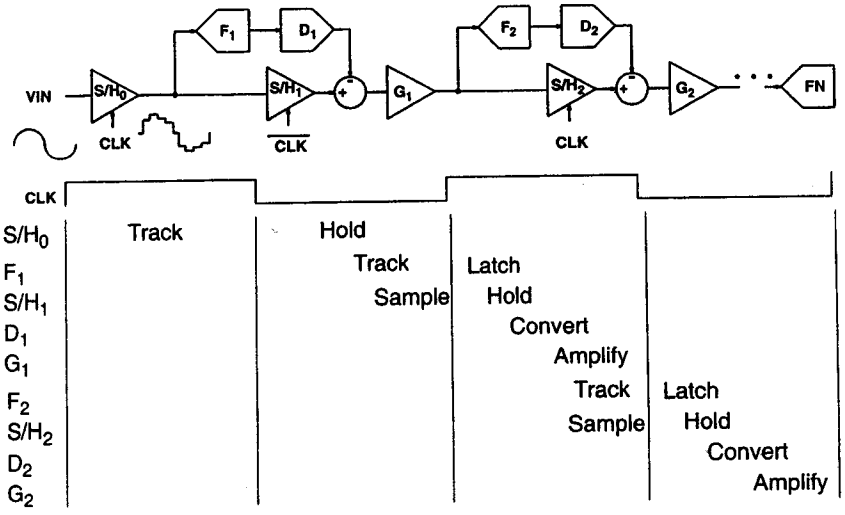
+ FURTHER REDUCTION IN # AND ACCURACY OF COMPS
+ ACCURACY DECREASES FOR 2ND STAGE, FURTHER FOR 3RD STAGE
- NEED ACCURATE DAC, SUBTRACTOR
- NEED TO WAIT FOR STAGE1 + STAGE2 + STAGE3+ . . .

Pipelined Architecture



+ NO WAITING (DECOUPLES CONVERSION RATE FROM CONVERSION TIME)
- REQUIRES SAMPLE/HOLD AMPLIFIERS BETWEEN STAGES

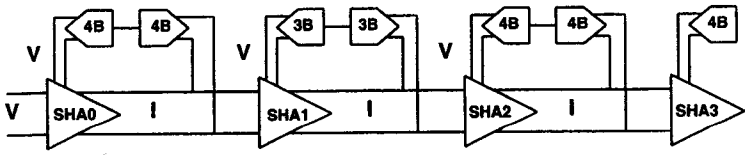
Pipeline Timing (SC Implementation)



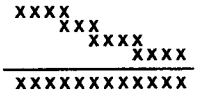
Key Points

- DAC, Subtractor, and Gain Allow Reduction of Number and Accuracy of Comparators
- Overlap Bits (Redundancy) for Flash Error Correction
- Errors Most Significant in First Stage
- Pipelining Decouples Conversion Rate From Conversion Time

12-Bit, 10MSPS ADC (AD872)



12-B ACCURATE 50NSEC | 9-B ACCURATE 50NSEC | 7-B ACCURATE 50NSEC | 4-B ACCURATE 50NSEC

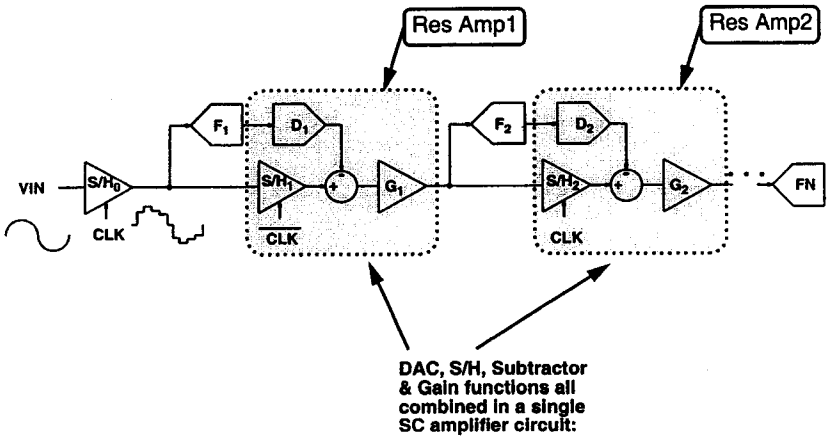


\+ MULTI-BIT, CURRENT-MODE ARCHITECTURE
\+ SUMMATION OF CURRENTS INHERENTLY LINEAR
\- NEED ACCURATE DAC AND SHA

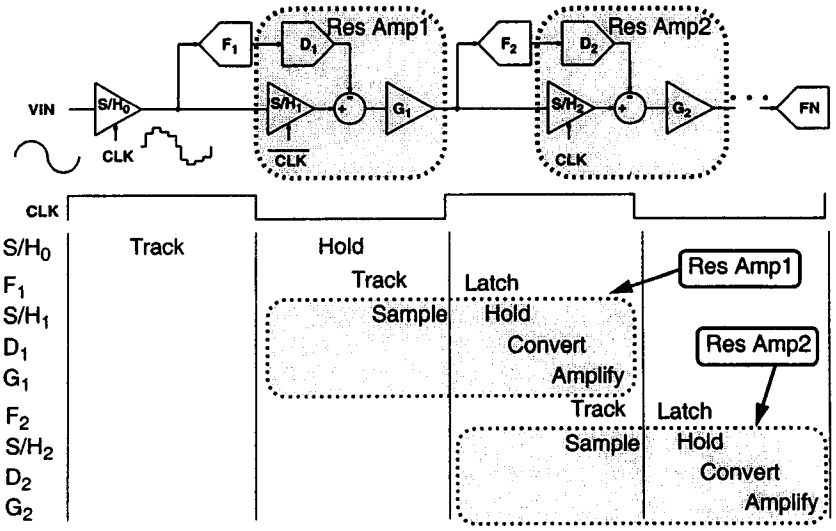
Outline

- Introduction/Background
- → Switched-Capacitor Implementation
- Switched-Capacitor Architecture Issues
- ADC Linearity
- Improving Linearity - Calibration
- Improving Linearity - Segmentation
- Residue Amplification
- Switched-Capacitor Sample/Hold Design
- Flash ADC Design
- Bench Evaluation/Characterization/Test
- 14bit 10MHz CMOS Pipelined ADC

Circuit Blocks Combined in a Single Switched-Capacitor Residue Amplification Stage

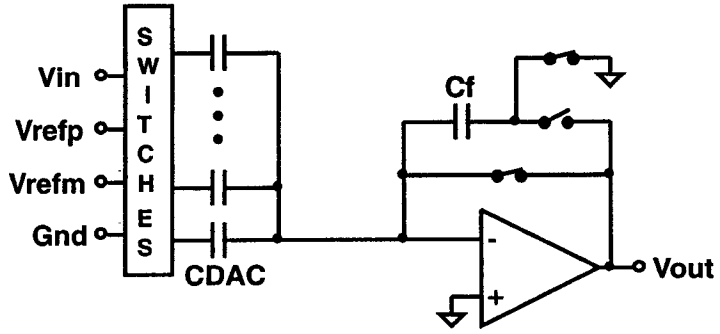


Timing of Switched-Cap Pipelined ADC

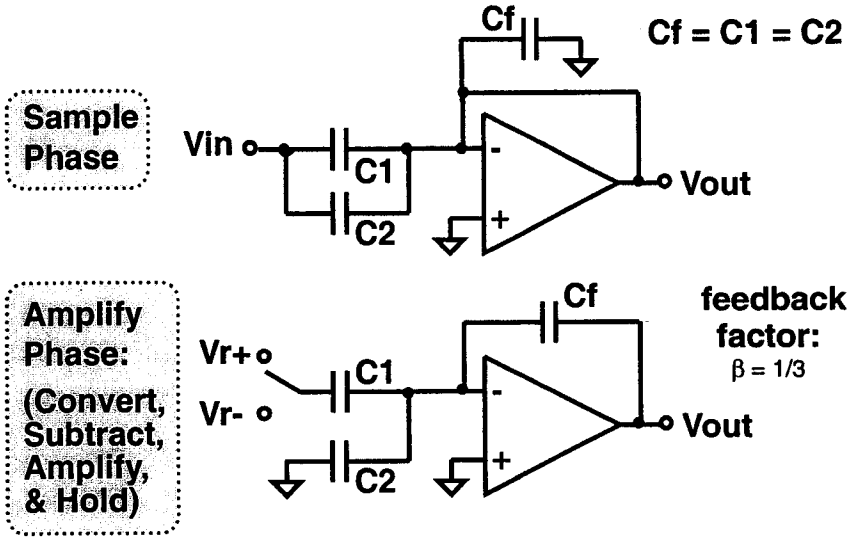


Switched-Capacitor Residue Circuit

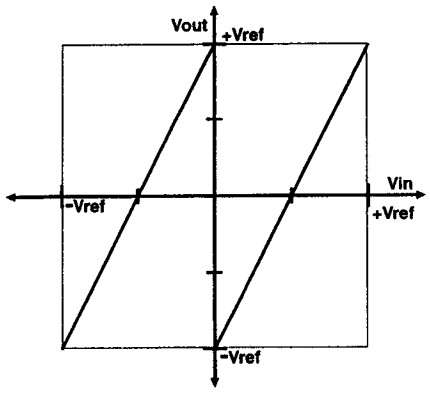
(DAC, subtract, gain, & S/H)



1-bit Switched-C Residue Circuit



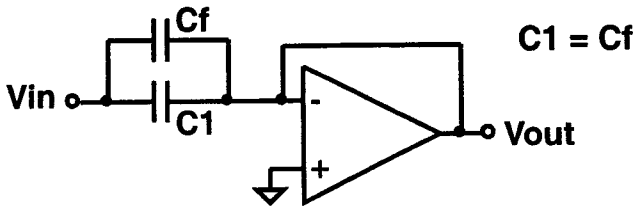
Transfer function of 1b Residue Circuit



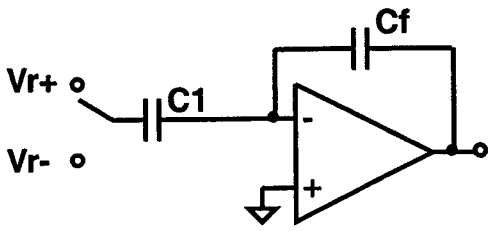
- Residue Gain = 2
- Comparator threshold at Vin = 0
- DAC capacitor C1 switches between +/- Vref

Improved 1-bit Switched-C Residue Circuit

Sample Phase

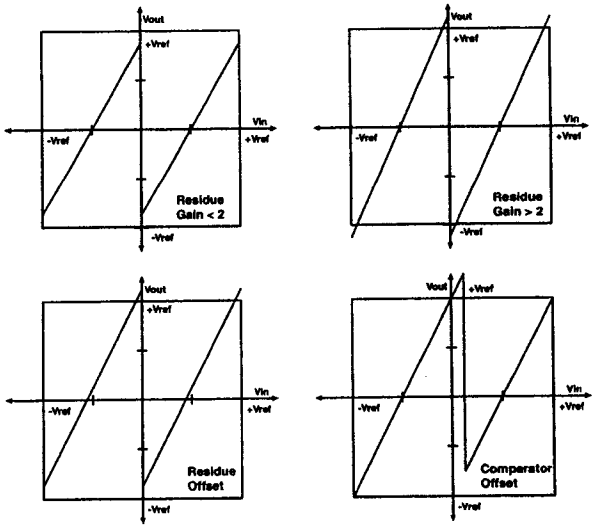


Amplify Phase:
(Convert, Subtract, Amplify, & Hold)



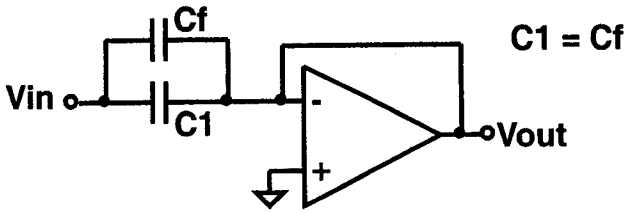
feedback factor:
$\beta = 1/2$

1b Residue with Amplifier & Comparator Errors

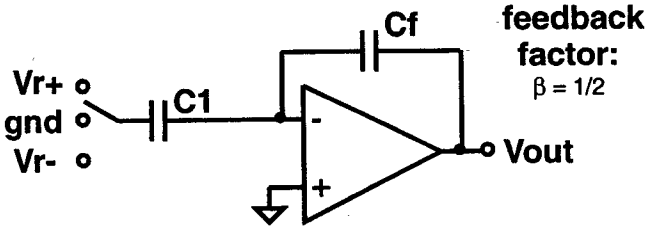


1.5-bit Switched-C Residue Circuit

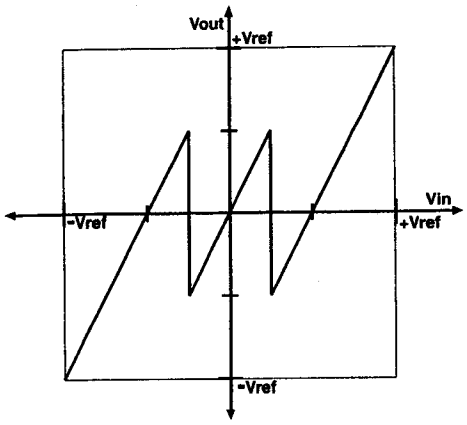
Sample Phase



Amplify Phase: (Convert, Subtract, Amplify, & Hold)

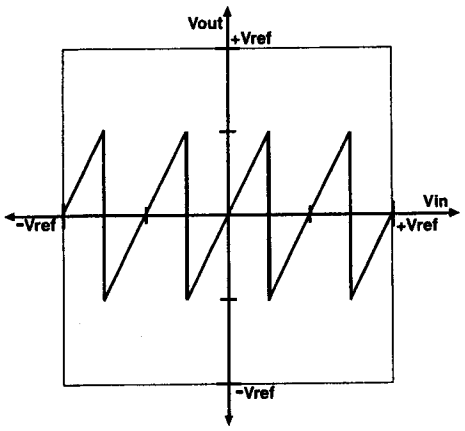


Transfer function of 1.5-bit Residue Circuit



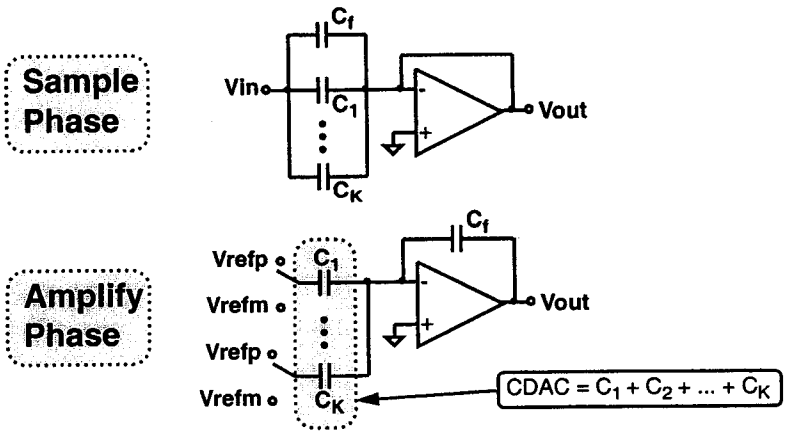
- Residue Gain = 2
- Comparator thresholds at +/-Vref/4
- 1 DAC capacitor switches between +Vref, gnd, -Vref

Transfer function of 2-bit Residue Circuit



- Residue Gain = 2
- Comparator thresholds at +/- Vref/4 and +/- 3Vref/4
- 4 DAC capacitors switch between +Vref & -Vref

Multi-bit Switched-C Residue Circuit



- Each additional DAC cap adds 1 more DAC level
- Amplifier gain proportional to ratio of C_f to CDAC

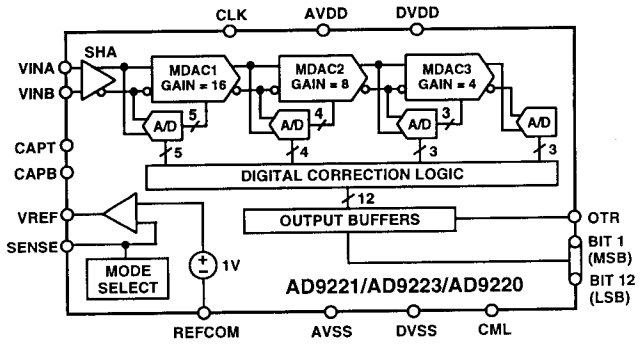
Complete 12-Bit 1.5/3.0/10.0 MSPS Monolithic A/D Converters

AD9221/AD9223/AD9220

FEATURES

Monolithic 12-Bit A/D Converter Product Family
Family Members Are: AD9221, AD9223, and AD9220
Flexible Sampling Rates: 1.5 MSPS, 3.0 MSPS and 10.0 MSPS
Low Power Dissipation: 59 mW, 100 mW and 250 mW
Single +5 V Supply
Integral Nonlinearity Error: 0.5 LSB
Differential Nonlinearity Error: 0.3 LSB
Input Referred Noise: 0.09 LSB
Complete: On-Chip Sample-and-Hold Amplifier and Voltage Reference
Signal-to-Noise and Distortion Ratio: 70 dB
Spurious-Free Dynamic Range: 86 dB
Out-of-Range Indicator
Straight Binary Output Data
28-Lead SOIC and 28-Lead SSOP

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD9221, AD9223, and AD9220 are a generation of high performance, single supply 12-bit analog-to-digital converters. Each device exhibits true 12-bit linearity and temperature drift performance[1] as well as 11.5 bit or better ac performance.[2] The AD9221/AD9223/AD9220 share the same interface options, package, and pinout. Thus, the product family provides an upward or downward component selection path based on performance, sample rate and power. The devices differ with respect to their specified sampling rate and power consumption which is reflected in their dynamic performance over frequency.

The AD9221/AD9223/AD9220 combine a low cost, high speed CMOS process and a novel architecture to achieve the resolution and speed of existing hybrid and monolithic implementations at a fraction of the power consumption and cost. Each device is a complete, monolithic ADC with an on-chip, high performance, low noise sample-and-hold amplifier and programmable voltage reference. An external reference can also be chosen to suit the dc accuracy and temperature drift requirements of the application. The devices use a multistage differential pipelined architecture with digital output error correction logic to provide 12-bit accuracy at the specified data rates and to guarantee no missing codes over the full operating temperature range.

The input of the AD9221/AD9223/AD9220 is highly flexible, allowing for easy interfacing to imaging, communications, medical, and data-acquisition systems. A truly differential input structure allows for both single-ended and differential input interfaces of varying input spans. The sample-and-hold (SHA) amplifier is equally suited for both multiplexed systems that switch full-scale voltage levels in successive channels as well as sampling single-channel inputs at frequencies up to and beyond the Nyquist rate. Also, the AD9221/AD9223/AD9220 is well suited for communication systems employing Direct-IF Down Conversion since the SHA in the differential input mode can achieve excellent dynamic performance *far beyond* its specified Nyquist frequency.[2]

A single clock input is used to control all internal conversion cycles. The digital output data is presented in straight binary output format. An out-of-range (OTR) signal indicates an overflow condition which can be used with the most significant bit to determine low or high overflow.

PRODUCT HIGHLIGHTS

The AD9221/AD9223/AD9220 family offers a complete single-chip sampling 12-bit, analog-to-digital conversion function in pin-compatible 28-lead SOIC and SSOP packages.

Flexible Sampling Rates—The AD9221, AD9223 and AD9220 offer sampling rates of 1.5 MSPS, 3.0 MSPS and 10.0 MSPS, respectively.

Low Power and Single Supply—The AD9221, AD9223 and AD9220 consume only 59 mW, 100 mW and 250 mW, respectively, on a single +5 V power supply.

Excellent DC Performance Over Temperature—The AD9221/AD9223/AD9220 provide 12-bit linearity and temperature drift performance.[1]

Excellent AC Performance and Low Noise—The AD9221/AD9223/AD9220 provides better than 11.3 ENOB performance and has an input referred noise of 0.09 LSB rms.[2]

Flexible Analog Input Range—The versatile onboard sample-and-hold (SHA) can be configured for either single ended or differential inputs of varying input spans.

NOTES
[1]Excluding internal voltage reference.
[2]Depends on the analog input configuration.

REV. D

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AD9221/AD9223/AD9220–SPECIFICATIONS

DC SPECIFICATIONS (AVDD = +5 V, DVDD = +5 V, f_{SAMPLE} = Max Conversion Rate, V_{REF} = 2.5 V, VINB = 2.5 V, T_{MIN} to T_{MAX} unless otherwise noted)

Parameter	AD9221	AD9223	AD9220	Units
RESOLUTION	12	12	12	Bits min
MAX CONVERSION RATE	1.5	3	10	MHz min
INPUT REFERRED NOISE (TYP)				
V_{REF} = 1 V	0.23	0.23	0.23	LSB rms typ
V_{REF} = 2.5 V	0.09	0.09	0.09	LSB rms typ
ACCURACY				
Integral Nonlinearity (INL)	±0.4	±0.5	±0.5	LSB typ
	±1.25	±1.25	±1.25	LSB max
Differential Nonlinearity (DNL)	±0.3	±0.3	±0.3	LSB typ
	±0.75	±0.75	±0.75	LSB max
INL[1]	±0.6	±0.6	±0.7	LSB typ
DNL[1]	±0.3	±0.3	±0.35	LSB typ
No Missing Codes	12	12	12	Bits Guaranteed
Zero Error (@ +25°C)	±0.3	±0.3	±0.3	% FSR max
Gain Error (@ +25°C)[2]	±1.5	±1.5	±1.5	% FSR max
Gain Error (@ +25°C)[3]	±0.75	±0.75	±0.75	% FSR max
TEMPERATURE DRIFT				
Zero Error	±2	±2	±2	ppm/°C typ
Gain Error[2]	±26	±26	±26	ppm/°C typ
Gain Error[3]	±0.4	±0.4	±0.4	ppm/°C typ
POWER SUPPLY REJECTION				
AVDD, DVDD (+5 V ± 0.25 V)	±0.06	±0.06	±0.06	% FSR max
ANALOG INPUT				
Input Span (with V_{REF} = 1.0 V)	2	2	2	V p-p min
(with V_{REF} = 2.5 V)	5	5	5	V p-p max
Input (VINA or VINB) Range	0	0	0	V min
	AVDD	AVDD	AVDD	V max
Input Capacitance	16	16	16	pF typ
INTERNAL VOLTAGE REFERENCE				
Output Voltage (1 V Mode)	1	1	1	Volts typ
Output Voltage Tolerance (1 V Mode)	±14	±14	±14	mV max
Output Voltage (2.5 V Mode)	2.5	2.5	2.5	Volts typ
Output Voltage Tolerance (2.5 V Mode)	±35	±35	±35	mV max
Load Regulation[4]	2.0	2.0	2.0	mV max
REFERENCE INPUT RESISTANCE	5	5	5	kΩ typ
POWER SUPPLIES				
Supply Voltages				
AVDD	+5	+5	+5	V (±5% AVDD Operating)
DVDD	+2.7 to +5.25	+2.7 to +5.25	+5 (±5%)	V
Supply Current				
IAVDD	14.0	26	58	mA max
	11.8	20	48	mA typ
IDVDD	0.5	0.5	12	mA max
	0.02	0.02	10	mA typ
POWER CONSUMPTION	59.0	100	250	mW typ
	70.0	130	310	mW max

NOTES
[1]V_{REF} = 1 V.
[2]Including internal reference.
[3]Excluding internal reference.
[4]Load regulation with 1 mA load current (in addition to that required by the AD9220/AD9221/AD9223).

Specification subject to change without notice.

AC SPECIFICATIONS (AVDD = +5 V, DVDD= +5 V, f_{SAMPLE} = Max Conversion Rate, V_{REF} = 1.0 V, VINB = 2.5 V, DC Coupled/Single-Ended Input T_{MIN} to T_{MAX} unless otherwise noted)

Parameters	AD9221	AD9223	AD9220	Units
MAX CONVERSION RATE	1.5	3.0	10.0	MHz min
DYNAMIC PERFORMANCE				
Input Test Frequency 1 (VINA = –0.5 dBFS)	100	500	1000	kHz
Signal-to-Noise and Distortion (SINAD)	70.0	70.0	70	dB typ
	69.0	68.5	68.5	dB min
Effective Number of Bits (ENOBs)	11.3	11.3	11.3	dB typ
	11.2	11.1	11.1	dB min
Signal-to-Noise Ratio (SNR)	70.2	70.0	70.2	dB typ
	69.0	68.5	69.0	dB min
Total Harmonic Distortion (THD)	–83.4	–83.4	–83.7	dB typ
	–77.5	–76.0	–76.0	dB max
Spurious Free Dynamic Range (SFDR)	86.0	87.5	88.0	dB typ
	79.0	77.5	77.5	dB max
Input Test Frequency 2 (VINA = –0.5 dBFS)	0.50	1.50	5.0	MHz
Signal-to-Noise and Distortion (SINAD)	69.9	69.4	67.0	dB typ
	69.0	68.0	65.0	dB min
Effective Number of Bits (ENOBs)	11.3	11.2	10.8	dB typ
	11.2	11.1	10.5	dB min
Signal-to-Noise Ratio (SNR)	70.1	69.7	68.8	dB typ
	69.0	68.5	67.5	dB min
Total Harmonic Distortion (THD)	–83.4	–82.9	–72.0	dB typ
	–77.5	–75.0	–68.0	dB max
Spurious Free Dynamic Range (SFDR)	86.0	85.7	75.0	dB typ
	79.0	76.0	69.0	dB max
Full Power Bandwidth	25	40	60	MHz typ
Small Signal Bandwidth	25	40	60	MHz typ
Aperture Delay	1	1	1	ns typ
Aperture Jitter	4	4	4	ps rms typ
Acquisition to Full-Scale Step	125	43	30	ns typ

Specifications subject to change without notice.

DIGITAL SPECIFICATIONS (AVDD = +5 V, DVDD = +5 V, T_{MIN} to T_{MAX} unless otherwise noted)

Parameters	Symbol		Units
CLOCK INPUT			
High Level Input Voltage	V_{IH}	+3.5	V min
Low Level Input Voltage	V_{IL}	+1.0	V max
High Level Input Current (V_{IN} = DVDD)	I_{IH}	±10	μA max
Low Level Input Current (V_{IN} = 0 V)	I_{IL}	±10	μA max
Input Capacitance	C_{IN}	5	pF typ
LOGIC OUTPUTS			
DVDD = 5 V			
High Level Output Voltage (I_{OH} = 50 μA)	V_{OH}	+4.5	V min
High Level Output Voltage (I_{OH} = 0.5 mA)	V_{OH}	+2.4	V min
Low Level Output Voltage (I_{OL} = 1.6 mA)	V_{OL}	+0.4	V max
Low Level Output Voltage (I_{OL} = 50 μA)	V_{OL}	+0.1	V max
DVDD = 3 V			
High Level Output Voltage (I_{OH} = 50 μA)	V_{OH}	+2.95	V min
High Level Output Voltage (I_{OH} = 0.5 mA)	V_{OH}	+2.80	V min
Low Level Output Voltage (I_{OL} = 1.6 mA)	V_{OL}	+0.4	V max
Low Level Output Voltage (I_{OL} = 50 μA)	V_{OL}	+0.05	V max
Output Capacitance	C_{OUT}	5	pF typ

Specifications subject to change without notice.

SWITCHING SPECIFICATIONS (T_{MIN} to T_{MAX} with AVDD = +5 V, DVDD = +5 V, C_L = 20 pF)

Parameters	Symbol	AD9221	AD9223	AD9220	Units
Clock Period[1]	t_C	667	333	100	ns min
CLOCK Pulsewidth High	t_{CH}	300	150	45	ns min
CLOCK Pulsewidth Low	t_{CL}	300	150	45	ns min
Output Delay	t_{OD}	8	8	8	ns min
		13	13	13	ns typ
		19	19	19	ns max
Pipeline Delay (Latency)		3	3	3	Clock Cycles

NOTES
[1]The clock period may be extended to 1 ms without degradation in specified performance @ +25 °C.
Specifications subject to change without notice.

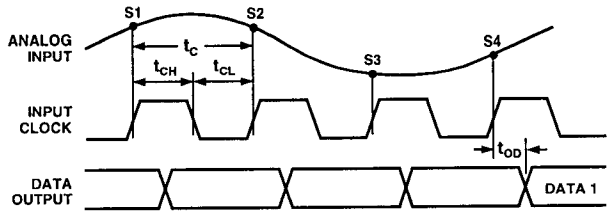


Figure 1. Timing Diagram

ABSOLUTE MAXIMUM RATINGS*

Parameter	With Respect to	Min	Max	Units
AVDD	AVSS	–0.3	+6.5	V
DVDD	DVSS	–0.3	+6.5	V
AVSS	DVSS	–0.3	+0.3	V
AVDD	DVDD	–6.5	+6.5	V
REFCOM	AVSS	–0.3	+0.3	V
CLK	AVSS	–0.3	AVDD + 0.3	V
Digital Outputs	DVSS	–0.3	DVDD + 0.3	V
VINA, VINB	AVSS	–0.3	AVDD + 0.3	V
VREF	AVSS	–0.3	AVDD + 0.3	V
SENSE	AVSS	–0.3	AVDD + 0.3	V
CAPB, CAPT	AVSS	–0.3	AVDD + 0.3	V
Junction Temperature			+150	°C
Storage Temperature		–65	+150	°C
Lead Temperature (10 sec)			+300	°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may effect device reliability.

THERMAL CHARACTERISTICS

Thermal Resistance
28-Lead SOIC
θ_{JA} = 71.4°C/W
θ_{JC} = 23°C/W
28-Lead SSOP
θ_{JA} = 63.3°C/W
θ_{JC} = 23°C/W

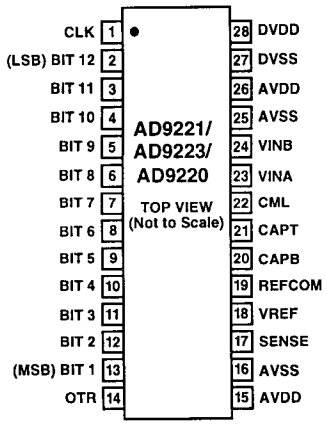
ORDERING GUIDE

Model	Temperature Range	Package Description	Package Options
AD9221AR	–40°C to +85°C	28-Lead SOIC	R-28
AD9223AR	–40°C to +85°C	28-Lead SOIC	R-28
AD9220AR	–40°C to +85°C	28-Lead SOIC	R-28
AD9221ARS	–40°C to +85°C	28-Lead SSOP	RS-28
AD9223ARS	–40°C to +85°C	28-Lead SSOP	RS-28
AD9220ARS	–40°C to +85°C	28-Lead SSOP	RS-28
AD9220/AD9221/AD9223SOICEB		Evaluation Board	
AD9220/AD9221/AD9223SSOPEB		Evaluation Board	

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although these devices feature proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONNECTIONS



PIN FUNCTION DESCRIPTIONS

Pin Number	Name	Description
1	CLK	Clock Input Pin
2	BIT 12	Least Significant Data Bit (LSB)
3–12	BIT N	Data Output Bit
13	BIT 1	Most Significant Data Bit (MSB)
14	OTR	Out of Range
15, 26	AVDD	+5 V Analog Supply
16, 25	AVSS	Analog Ground
17	SENSE	Reference Select
18	VREF	Reference I/O
19	REFCOM	Reference Common
20	CAPB	Noise Reduction Pin
21	CAPT	Noise Reduction Pin
22	CML	Common-Mode Level (Midsupply)
23	VINA	Analog Input Pin (+)
24	VINB	Analog Input Pin (–)
27	DVSS	Digital Ground
28	DVDD	+3 V to +5 V Digital Supply

DEFINITIONS OF SPECIFICATION

INTEGRAL NONLINEARITY (INL)

INL refers to the deviation of each individual code from a line drawn from "negative full scale" through "positive full scale." The point used as "negative full scale" occurs 1/2 LSB before the first code transition. "Positive full scale" is defined as a level 1 1/2 LSB beyond the last code transition. The deviation is measured from the middle of each particular code to the true straight line.

DIFFERENTIAL NONLINEARITY (DNL, NO MISSING CODES)

An ideal ADC exhibits code transitions that are exactly 1 LSB apart. DNL is the deviation from this ideal value. Guaranteed no missing codes to 12-bit resolution indicates that all 4096 codes, respectively, must be present over all operating ranges.

ZERO ERROR

The major carry transition should occur for an analog value 1/2 LSB below VINA = VINB. Zero error is defined as the deviation of the actual transition from that point.

GAIN ERROR

The first code transition should occur at an analog value 1/2 LSB above negative full scale. The last transition should occur at an analog value 1 1/2 LSB below the nominal full scale. Gain error is the deviation of the actual difference between first and last code transitions and the ideal difference between first and last code transitions.

TEMPERATURE DRIFT

The temperature drift for zero error and gain error specifies the maximum change from the initial (+25°C) value to the value at T_{MIN} or T_{MAX}.

POWER SUPPLY REJECTION

The specification shows the maximum change in full scale from the value with the supply at the minimum limit to the value with the supply at its maximum limit.

APERTURE JITTER

Aperture jitter is the variation in aperture delay for successive samples and is manifested as noise on the input to the A/D.

APERTURE DELAY

Aperture delay is a measure of the sample-and-hold amplifier (SHA) performance and is measured from the rising edge of the clock input to when the input signal is held for conversion.

SIGNAL-TO-NOISE AND DISTORTION (S/N+D, SINAD) RATIO

S/N+D is the ratio of the rms value of the measured input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for S/N+D is expressed in decibels.

EFFECTIVE NUMBER OF BITS (ENOB)

For a sine wave, SINAD can be expressed in terms of the number of bits. Using the following formula,

$$N = (SINAD - 1.76)/6.02$$

it is possible to get a measure of performance expressed as N, the effective number of bits.

Thus, effective number of bits for a device for sine wave inputs at a given input frequency can be calculated directly from its measured SINAD.

TOTAL HARMONIC DISTORTION (THD)

THD is the ratio of the rms sum of the first six harmonic components to the rms value of the measured input signal and is expressed as a percentage or in decibels.

SIGNAL-TO-NOISE RATIO (SNR)

SNR is the ratio of the rms value of the measured input signal to the rms sum of all other spectral components below the Nyquist frequency, excluding the first six harmonics and dc. The value for SNR is expressed in decibels.

SPURIOUS FREE DYNAMIC RANGE (SFDR)

SFDR is the difference in dB between the rms amplitude of the input signal and the peak spurious signal.

AD9221–Typical Characterization Curves (AVDD = +5 V, DVDD = +5 V, f_{SAMPLE} = 1.5 MSPS, T_A = +25°C)

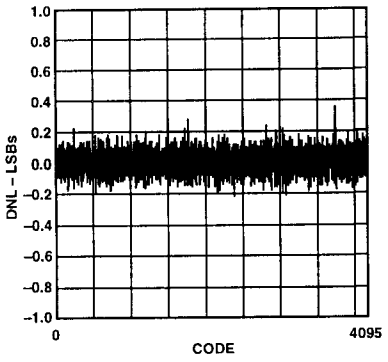


Figure 2. Typical DNL

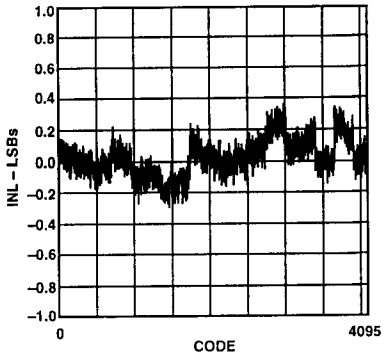


Figure 3. Typical INL

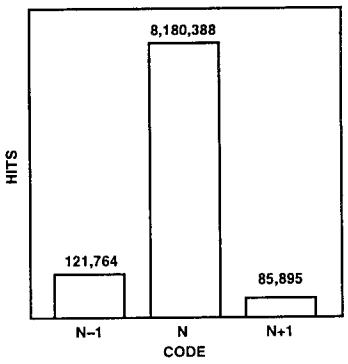


Figure 4. "Grounded-Input" Histogram (Input Span = 2 V p-p)

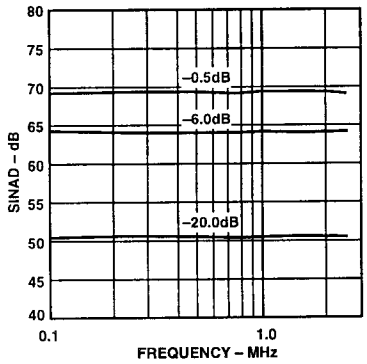


Figure 5. SINAD vs. Input Frequency (Input Span = 2.0 V p-p, V_{CM} = 2.5 V)

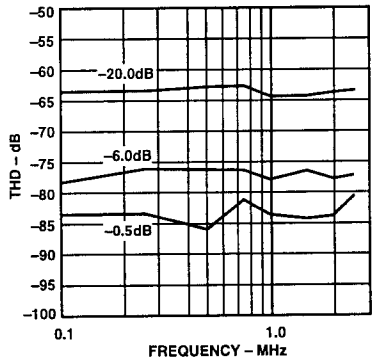


Figure 6. THD vs. Input Frequency (Input Span = 2.0 V p-p, V_{CM} = 2.5 V)

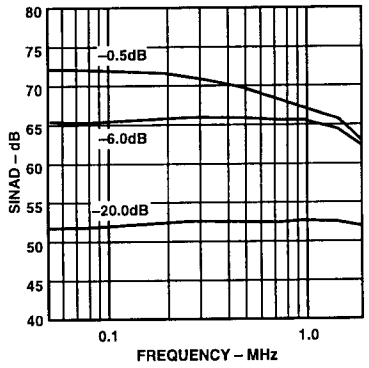


Figure 7. SINAD vs. Input Frequency (Input Span = 5.0 V p-p, V_{CM} = 2.5 V)

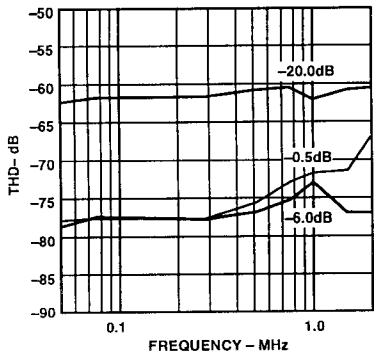


Figure 8. THD vs. Input Frequency (Input Span = 5.0 V p-p, V_{CM} = 2.5 V)

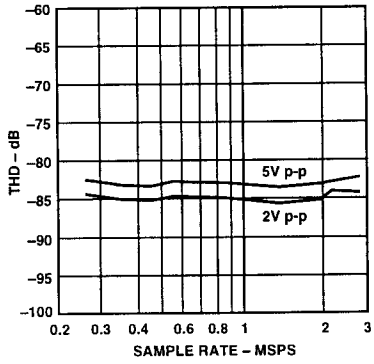


Figure 9. THD vs. Sample Rate (A_{IN} = –0.5 dB, f_{IN} = 500 kHz, V_{CM} = 2.5 V)

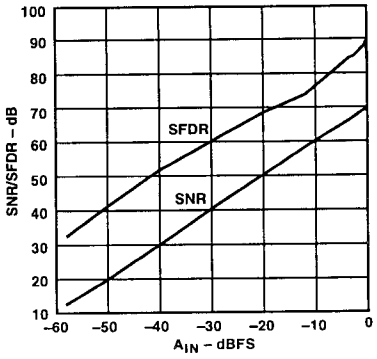


Figure 10. SNR/SFDR vs. A_{IN} (Input Amplitude) (f_{IN} = 500 kHz, Input Span = 2 V p-p, V_{CM} = 2.5 V)